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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/041,863	10/22/2001	Ikuroh Ichitsubo	21MMC-10	5392

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EXAMINER
PATEL, ISHWARBHAI B

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 12/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/041,863	ICHITSUBO ET AL.	
	Examiner	Art Unit	
	Ishwar (I. B.) Patel	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-28 is/are pending in the application.

4a) Of the above claim(s) 28 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-27 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on 22 October 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claim 1-27, drawn to a radio frequency amplifier module, classified in class 174, subclass 260.

   II. Claim 28, drawn to a method of making a radio frequency, classified in class 29, subclass 832.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by another and materially different process such as the well and ledge can be formed in individual circuit board before laminating together. Further, the bottom plate can be glued to the board instead of lamination.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, and the search required for Group II is not required for Group I, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Francis L. Conte (29,630) on November 25, 2002, a provisional election was made with traverse to prosecute the invention of a radio frequency amplifier module, claims 1-27. Affirmation of this election must be made by applicant in replying to this Office action. Claim 28 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thaler et al., US Patent No. 5,847,935, hereafter Thaler, in view of Yoshikawa et al., US Patent No. 5,796,165, hereafter Yoshikawa.

Regarding claim 1, Thaler discloses a radio frequency module comprising: a plurality of printed circuit boards laminated atop a bottom conductor plate, and including a radio frequency semiconductor chip mounted in a well extending through said boards in electrical connection therewith and electrically bonded atop said plate (package 10 with a metallic base plate 12 and body 16 of electrically insulating material and electronic circuit component 30, see figure 1 and 2, column1 line 57 to column 2, line 35, including electrical connection of the component, see figure 3, column 3, line 50-55), except explicitly disclosing the device is semiconductor amplifier chip. However such high frequency semiconductor chip with amplifier are known in the art and apparently used for amplifying input / out put signals. Yoshikawa discloses one such IC device for use in radio systems such as mobile communications. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the electronic circuit chip package of Thaler with semiconductor amplifier chip, as taught by Yoshikawa, apparently, in order to amplify input / output signal.

Regarding claim 2, the combination of Thaler and Yoshikawa further discloses top terminals of the chip electrically joined to one of said board, and a metallized base directly bonded atop said plate (see Thaler figure 1, 2 and 3).

Regarding claim 3, 4 and 5, the combination of Thaler and Yoshikawa further disclose the top boards and intermediate laminates including the input and output impedance matching circuit as disclosed by Yoshikawa.

Regarding claim 6, the combination of Thaler and Yoshikawa further discloses metal layers for providing grounding for the module, Thaler, column 2, line 50-55.

Regarding claim 7, the combination of Thaler and Yoshikawa further discloses the electrically conductive terminals, see Thaler figure 1.

Regarding claim 8, the combination of Thaler and Yoshikawa further discloses the bottom plate is a ground for the chip and the printed circuits, see Thaler figure 1, 2 and 3, conductive layer 20, connecting the base plate, column 1, line 60 to column 2, line 25.

Regarding claims 9-11, the combination of Thaler and Yoshikawa further discloses the ledge surrounding the chip with electrical connection, including the well as shown in, Thaler, figure 1, 2 and 3 and Yoshikawa figure 1.

Regarding claim claims 12 and 13, the combination of Thaler and Yoshikawa does not explicitly disclose the five terminals for input / output connection, however, it is

inherent to have the required number of terminals for the connections and how the chips can be configured to get the desired function of the device. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the electronic circuit chip package of the combination of Thaler and Yoshikawa with five terminals, in order to have the required input / output connections.

Regarding claim 14, the combination of Thaler and Yoshikawa disclose the bottom plate underlies substantially all of said bottom board. Though, the combination of Thaler and Yoshikawa does not disclose the chip comprises Gallium Arsenide Heterojunction Bipolar Transistor, such transistor are known in the art and can be used depending upon the system requirement. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the electronic circuit chip package of the combination of Thaler and Yoshikawa with Gallium Arsenide Heterojunction Bipolar Transistor in order to have improved efficiency and overall performance of the amplifier system.

Regarding claims 15 and 18, the combination of Thaler and Yoshikawa discloses the metal cover on the top of the board and the well, see Yoshikawa figure 1.

Regarding claim 16, the combination of Thaler and Yoshikawa further discloses metal sidewalls surrounding the said laminated boards, see Yoshikawa figure 1.

Regarding claim 17, the combination of Thaler and Yoshikawa further disclose metal cover and sidewall as disclosed by Yoshikawa and the bottom conductor plate as shown by Thaler covering the semiconductor chip.

Regarding claim 19 and 20, though the combination of Thaler and Yoshikawa does not disclose the top cover electrically grounded, such grounding is known in the art for shielding the component. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the electronic circuit chip package of the combination of Thaler and Yoshikawa having top cover electrically grounded for shielding the components and providing shielding from all the side in combination with the bottom plate.

Regarding claims 21 –27, though the combination of Thaler and Yoshikawa does not disclose the cover board includes the dielectric substrate along with a circuit and components there on, the required components can be located in the board depending upon the space available and economic method to install the same. Further, the applicant is not disclosing any specific advantage of providing such cover with the substrate. Therefore, it would have been obvious to one having ordinary skill in the art to provide the combination of Thaler and Yoshikawa with the cover with the component to accommodate the required component into the assembly.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ishiwakawa et al.. discloses radio frequency module with semiconductor device thermally and electrically coupled to metal film.

Yoshikawa et al., discloses RF power amplifying circuit device.

Olofsson et al., discloses power transistor for radio frequency amplifier.

Laureanti discloses a power transistor device.

Ingram et al., discloses power amplifier network and discuss about the use of Gallium Arsenide transistor in the background discloser.

Harju discloses a package with component mounted on the cover above the chip cavity.

Weber, Soderholm, Karnezos and Hamzehwhdoost et al., discloses packages having chip mounted in the cavity with cooling means.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel, whose telephone number is (703) 305 2617. The examiner can normally be reached on M-F (6:30 - 4) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L Talbott can be reached on (703) 305 9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305 3431 for regular communications and (703) 305 7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 0956.

ibp
December 11, 2002

12-13-02

ALBERT W. PALADINI
PRIMARY EXAMINER